AN3594K

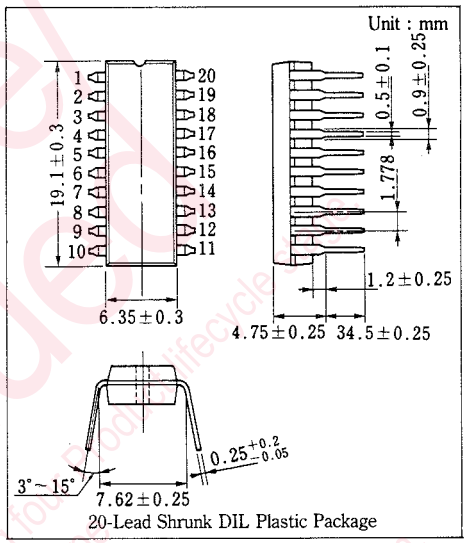
VTR Color Signal Alignment Correction Circuit

■ Outline

The AN3594K is an integrated circuit designed for correcting the signal alignment for special playback in PAL long-time mode.

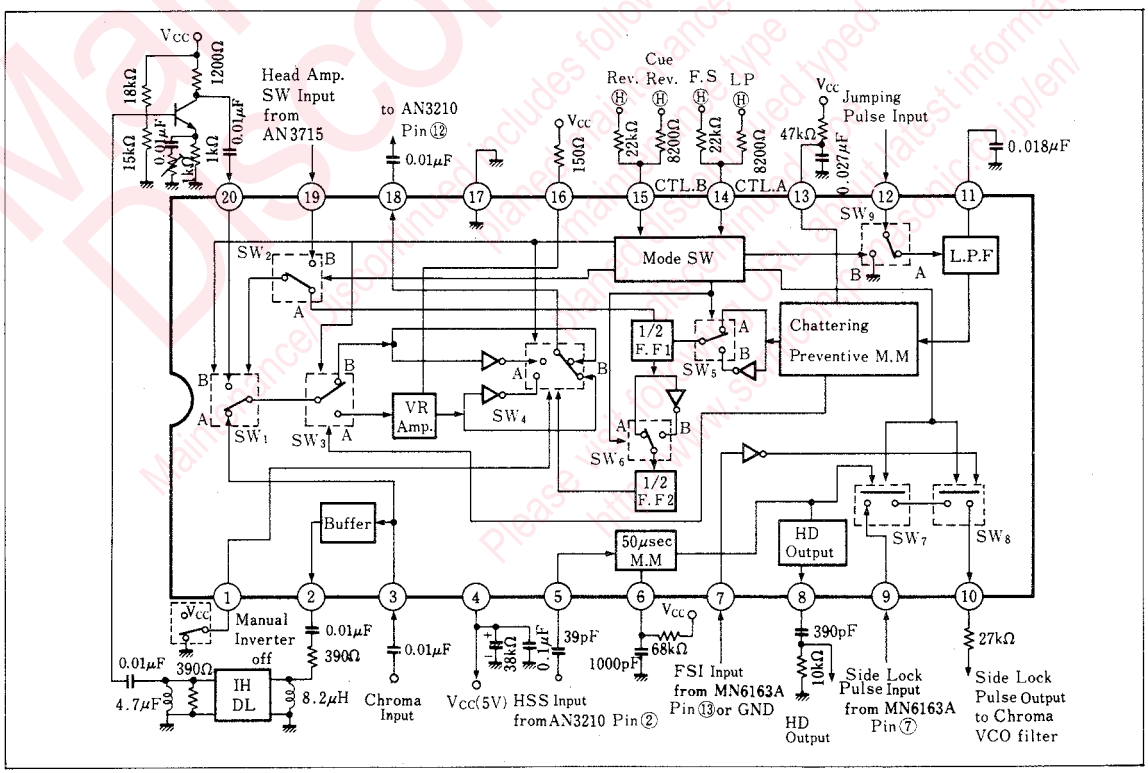
■ Features

- Applicable to Review and Field-still modes.
- Stable tint characteristics by variable amplifier.
- Supply voltage : V_{CC}=5V



20-Lead Shrunk DIL Plastic Package

■ Block Diagram



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■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Inverter off	11	Noise Preventive External
2	Chroma Buffer Output	12	Jumping Pulse Input
3	Chroma Input	13	Chattering Preventive M.M. External
4	V_{CC}	14	SP/LP/F.S. SW
5	HSS Input	15	LP/Cue/Rev SW
6	50 μ s M.M External	16	Gain Adjust
7	FSI Pulse Input	17	GND
8	HD Output	18	Chroma Output
9	Side Lock Pulse Input	19	Head Amp. SW Pulse Input
10	Side Lock Pulse Output	20	1H Delay Signal Input

■ Absolute Maximum Ratings (Ta=25℃)

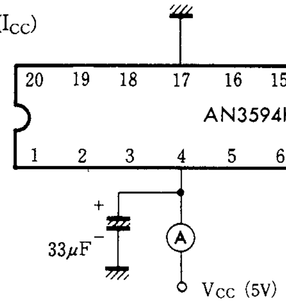
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6	V
Power Dissipation(Ta=70℃)	P_D	250	mW
Operating Ambient Temperature	T_{opr}	−20～+70	℃
Storage Temperature	T_{stg}	−55～+150	℃

■ Electrical Characteristics (Ta=25℃)

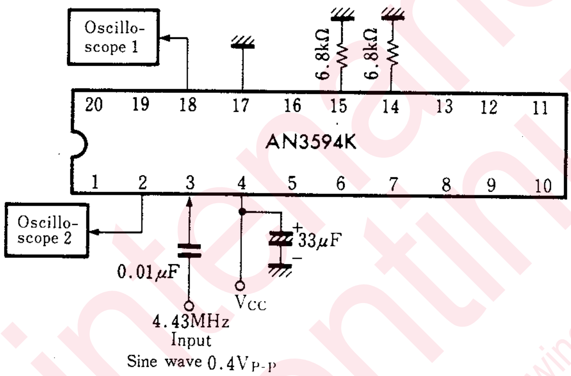
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I_{CC}	1	V_{CC}=5V	16		40	mA
Chroma Output Amplification (SP/LP Normal)	$v_{18\text{-}N}$	2	V_{CC}=5V, Pin③input, Chroma 0.4$V_{P\text{-}P}$	0.34		0.47	$v_{P\text{-}P}$
Buffer Amp. Output Amplification	v_2	2	V_{CC}=5V	0.34		0.47	$v_{P\text{-}P}$
Gain Adjustment Range	G_{16}	3	V_{CC}=5V	−3		2.5	dB
FSI Input Sensitivity	S_7	4	V_{CC}=5V	3.5			V
Chroma Output Amplification(IH Delay)	$v_{18\text{-}D}$	5	V_{CC}=5V, Pin⑳input, Chroma 0.4$V_{P\text{-}P}$	0.34		0.47	$v_{P\text{-}P}$
Chroma Output DC offset	V_{offset}	6	V_{CC}=5V, Pin⑫pulse input			100	mV
IH Delay/Normal Crosstalk	CT	7	V_{CC}=5V, Pin⑳input, Chroma 0.4$V_{P\text{-}P}$			−35	dB
Head Amp. Sw Pulse Input Sensitivity	S_{19}	7	V_{CC}=5V	3.5			V
Jumping Pulse Input Sensitivity	S_{12}	6	V_{CC}=5V	4.2			V
Inverter off Input Sensitivity	S_1	8	V_{CC}=5V	3.5			V
SP Mode Range	$S_{14\text{-}1}$	9	V_{CC}=5V			2	V
LP Normal Mode Range(1)	$S_{14\text{-}2}$	9	V_{CC}=5V	2.75		3.25	V
LP Still Mode Range	$S_{14\text{-}3}$	9	V_{CC}=5V	3.8		4.3	V
LP Normal Mode Range(2)	$S_{15\text{-}1}$	10	V_{CC}=5V			2	V
LP Cue Mode Range	$S_{15\text{-}2}$	10	V_{CC}=5V	2.75		3.25	V
LP Rev Mode Range	$S_{15\text{-}3}$	10	V_{CC}=5V	3.8		4.3	V
HSS Input Sensitivity	S_5	11	V_{CC}=5V	2			V
HSS M.M Width	$t_{W\text{-}8}$	11	V_{CC}=5V, R=68kΩ, C=1000pF	43		57	μs
HD Output Amplification	v_8	11	V_{CC}=5V			3.8	V
HSS M.M Pull-in Range	I_6	12	V_{CC}=5V	0.4		0.8	mA
Chattering Preventive M.M Pull-in Current	I_{13}	12	V_{CC}=5V	0.6		1.1	mA
Chattering Preventive M.M Width	$t_{W\text{-}13}$	13	V_{CC}=5V, R=47kΩ, C=0.027μF	1.3		2.1	ms
Side Lock Prevetive Pulse Flow-in Current	$I_{IN\text{-}10}$	13	V_{CC}=5V	2		6	mA
Side Lock Preventive Pulse	$I_{0\text{-}10}$	13	V_{CC}=5V	1		4	mA

Note : Operating Supply voltage range $V_{CC(opr)}$=4.5～5.5V

Test Circuit 1 (I_{CC})

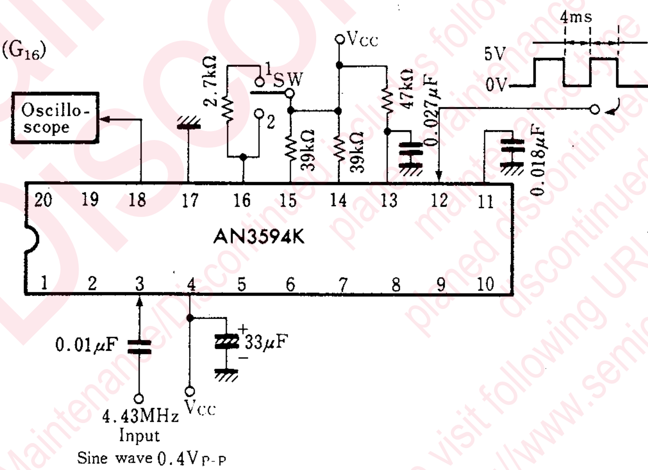


Test Circuit 2 ($v_{18\text{-}N}$, v_2)



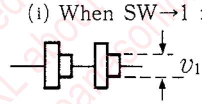
- v_{18-N}
  Oscilloscope 1 amplification
- v_2
  Oscilloscope 2 amplification

Test Circuit 3 (G_{16})



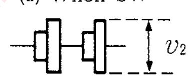
- G_{16}

(i) When SW→1 :



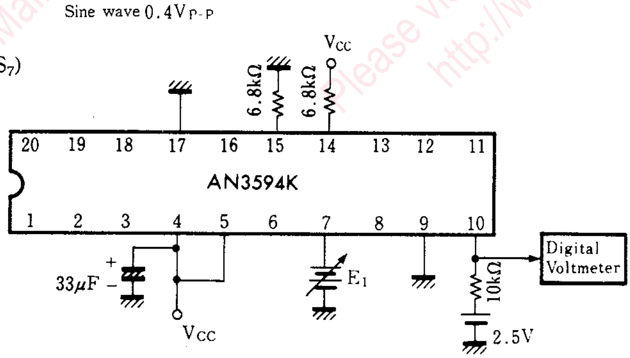
$$\text{Gain Low} = 20\log\frac{v_1}{0.4}$$

(ii) When SW → 2 :



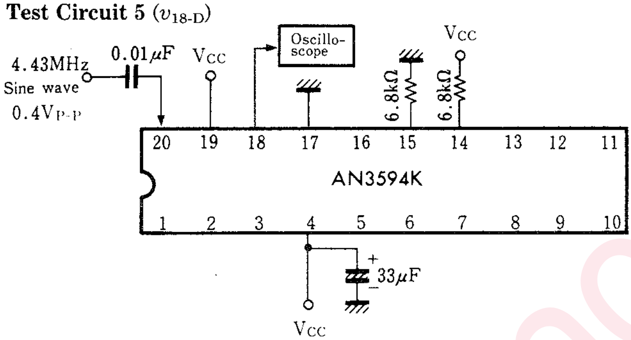
$$\text{Gain High} = 20\log\frac{v_2}{0.4}$$

Test Circuit 4 (S_7)

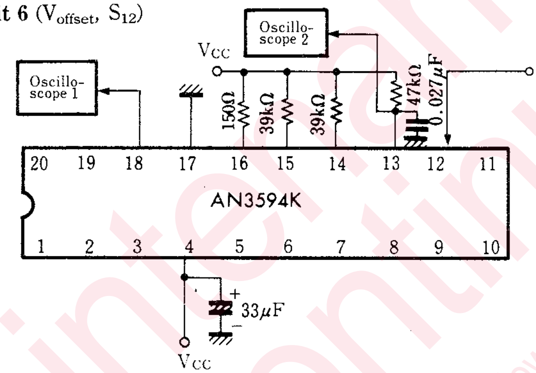


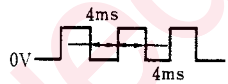
- S_7
  voltage when Pin ⑩ voltage increases from 0.5V or less to 2.5V, increasing E_1 voltage from 0V

Test Circuit 5 ($v_{18\text{-}D}$)



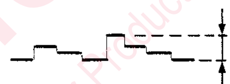
Test Circuit 6 (V_{offset}, S_{12})



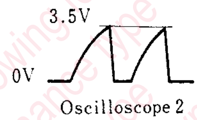


- **Voffset**

Oscilloscope 1 waveform for Pin ⑫ pulse amplification $5V_{O-P}$

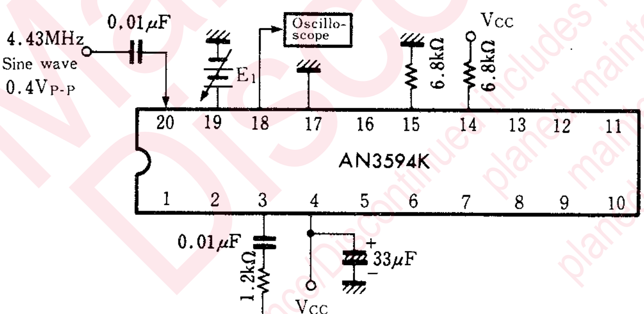


- **S_{12}**



Pin ⑫ pulse amplification position when a waveform as shown left appears at Pin ⑬, increasing Pin ⑫ input pulse amplification

Test Circuit 7 (CT, S_{19})



- **CT**

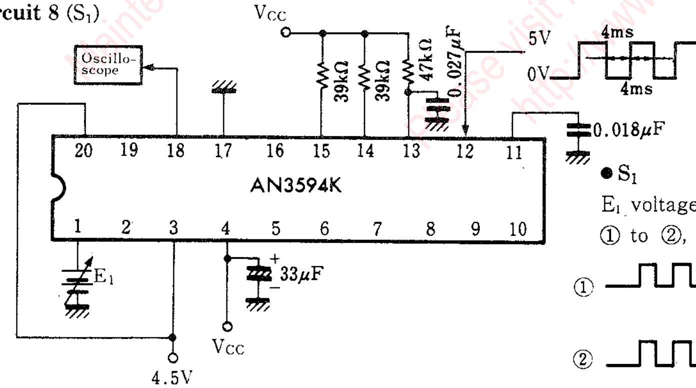
Assuming that oscilloscope amplification is v_1 when E_1= 0V, the following equation is established.

$$CT = 20\log\frac{v_1}{0.4V_{P\text{-}P}}$$

- **S_{19}**

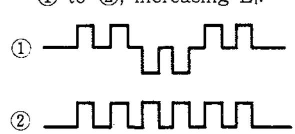
E_1 voltage when Pin ⑱ amplification is $0.3V_{P\text{-}P}$ or more, increaing E_1 from 0V

Test Circuit 8 (S_1)

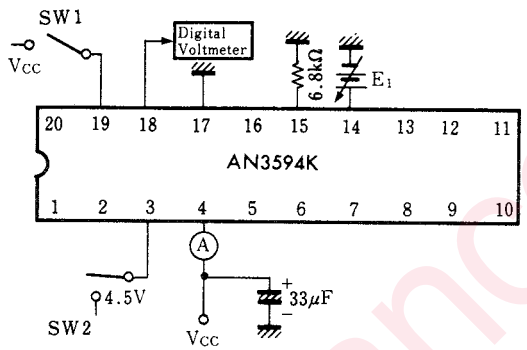


- **S_1**

E_1 voltage when Pin ⑱ output changes from ① to ②, increasing E_1.

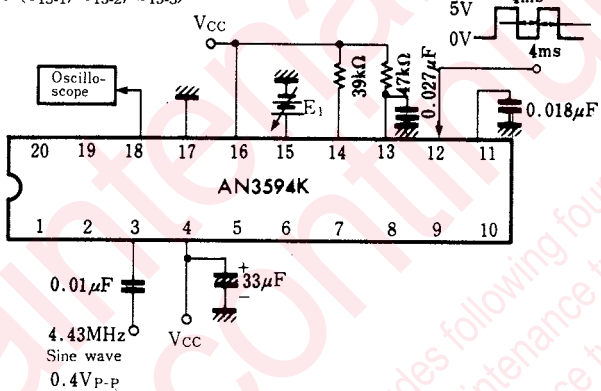


Test Circuit 9 (S_{14-1}, S_{14-2}, S_{14-3})

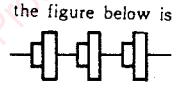


- S_{14-1} SW1→OPEN, SW2→OPEN
  Range until the current value reaches up to 0.8mA by increasing E_t from 0V
- S_{14-2} SW1→V_{CC}, SW2→4.5V
  Range Pin ⑱ voltage becomes 3.5V or less by increasing E_t from the upper limit value in SP mode
- S_{14-3} SW→V_{CC}, SW2→4.5V
  Range Pin ⑱ voltage becomes 3.5V or more by increasing E_t from the upper limit value in LP mode

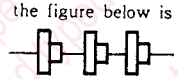
Test Circuit 10 (S_{15-1}, S_{15-2}, S_{15-3})



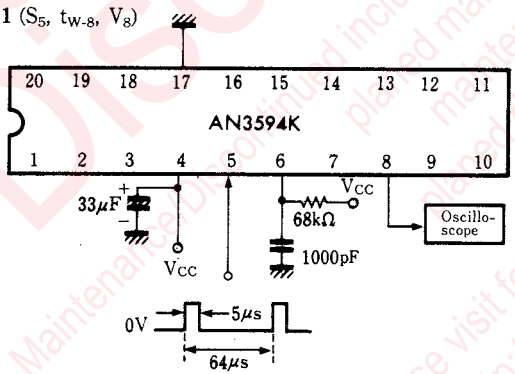
- S_{15-1}
  Range in which E_t increases from 0V and a continuous wave is generated
- S_{15-2}
  Range in which E_t increases and a waveform as shown in the figure below is generated



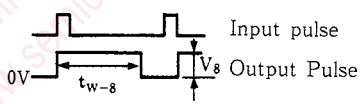
- S_{15-3}
  Range in which E_t increases and a waveform as shown in the figure below is generated



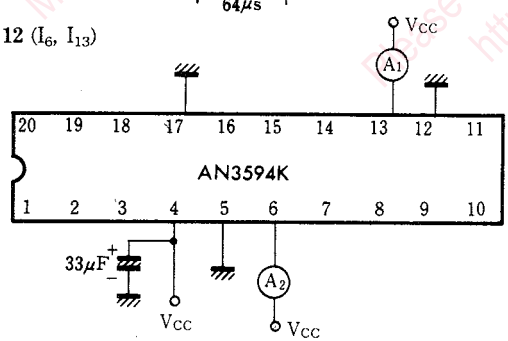
Test Circuit 11 (S_5, t_{W-8}, V_8)



- S_5
  When Pin ⑧ pulse amplification becomes 3.5V or more by increasing input pulse width
- t_{W-8}, V_8

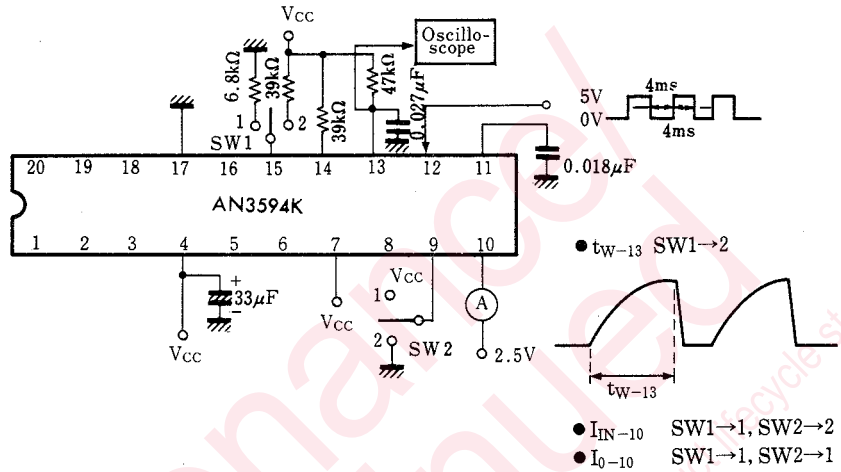


Test Circuit 12 (I_6, I_{13})

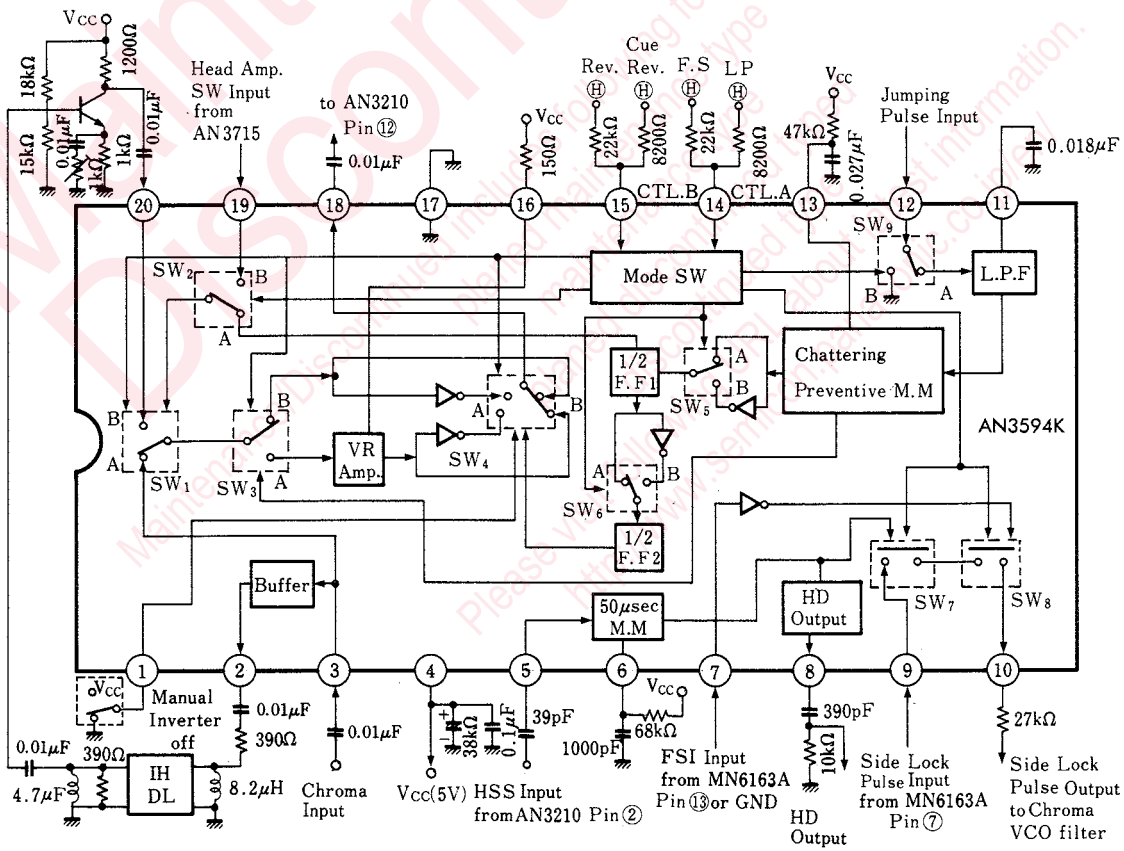


- $I_6 = A_2$
- $I_{13} = A_1$

Test Circuit 13 (t_{W-13}, I_{IN-10}, I_{O-10})



■ Application Circuit



■ Fuctional Explanation

Relationships between Pin⑭/⑮and Modes

Pin⑭Voltage / Pin⑮Voltage	L	M	H
L	SP	LP Normal	LP Still
M	SP	LP Cue	Disable Mode
H	SP	LP Rev	Disable Mode

Side Lock Pulse Operation for Special Characteristics

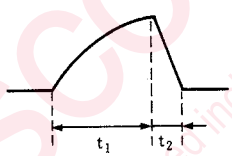
Pin⑦Voltage	Pin⑧Voltage	Pin⑩Output
L	L	M irrespective of Pin⑨input
L	H	Pin⑨Output to be made as it is
H	L	M irrespective of Pin⑨input
H	H	M irrespective of Pin⑨input

(Pin⑩ : M=1/2Vcc fixed)

SW Condition in Modes

	SP	LP Normal	LP Cue	LP Rev	LP Still
SW1	A	A	½ FF1 H→B L→A	½ FF1 H→B L→A	Pin⑲ H→B L→A
SW2	OPEN	OPEN	A	A	B
SW3	B	B	Pin⑫ H→A L→B	Pin⑫ H→A L→B	B
SW4	B	B	½ FF2 H→A L→B	½ FF2 H→A L→B	B
SW5	×	×	B	A	×
SW6	×	×	B	A	×
SW7	OFF	OFF	ON	ON	ON
SW8	OFF	OFF	ON	ON	ON
SW9	B	B	A	A	B

(1)50μsM.M external constant setting method



① Rise time

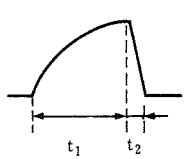
$t_1 = RC1n2$

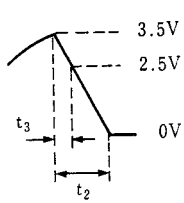
②Fall time

$$t_2 = RC\ 1n\frac{RI_O - \frac{1}{2}Vcc}{RI_O - Vcc}$$

(∵I_O: Pin ⑥ pull-in current)

(2) Chattering preventive M.M external constant setting method





① Rise time

$t_1 = RC1n3.3$(due to thresh electric potential=3.5V)

②Fall time

$$t_2 = RC\ 1n\frac{RI_O - 0.3Vcc}{RI_O - Vcc}$$

(∵I_O: Pin ⑬ pull-in current)

・Since t_3 pulse serves as control signal to decide whether good or bad in the fall time t_2, set as follows:

$t_2 \geqq 100\mu s$

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